

<b>Notice of Allowability</b>	Application No.	Applicant(s)
	10/612,371	VAN DER WAGT, JAN PAUL ANTHONIE
	Examiner My-Trang N. Ton	Art Unit 2816

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1.  This communication is responsive to 08/12/04.
2.  The allowed claim(s) is/are 1-4, 6, 8-26, 28-32, 34 and 36-42.
3.  The drawings filed on 02 July 2003 are accepted by the Examiner.
4.  Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  - a)  All
  - b)  Some\*
  - c)  None
 of the:
  1.  Certified copies of the priority documents have been received.
  2.  Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3.  Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.  
**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5.  A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
6.  CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.
  - (a)  including changes required by the Notice of Draftsperson's Patent Drawing Review ( PTO-948) attached
    - 1)  hereto or 2)  to Paper No./Mail Date \_\_\_\_\_.
  - (b)  including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7.  DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

#### Attachment(s)

1.  Notice of References Cited (PTO-892)
2.  Notice of Draftsperson's Patent Drawing Review (PTO-948)
3.  Information Disclosure Statements (PTO-1449 or PTO/SB/08),  
Paper No./Mail Date \_\_\_\_\_
4.  Examiner's Comment Regarding Requirement for Deposit  
of Biological Material
5.  Notice of Informal Patent Application (PTO-152)
6.  Interview Summary (PTO-413),  
Paper No./Mail Date \_\_\_\_\_.
7.  Examiner's Amendment/Comment
8.  Examiner's Statement of Reasons for Allowance
9.  Other \_\_\_\_\_.

***Reasons for allowance***

The following is an examiner's statement of reasons for allowance:

The present invention is drawn to an improved high-speed output buffer utilizing a cascode transistor module, a differential pair module, a pair of external load impedances, a resistive load, a cascode bias voltage, a bleed resistor and one or more inductive modules ... recited in claims 1-4, 6, 8-26, 28-32, 34 and 36-42. None of the prior art disclosed or suggested to show the particular structure and/or the particular operation recited in these claims namely: the combination of "the cascode transistor module", "the differential pair module", "cascode module connected to receive at its second current terminals ... and a second output waveform" and "engineering the resistive loads seen by the first terminals ... for each of said first output waveform and said second output waveform" as recited in claim 1; the combination of "the cascode transistor module", "the differential pair module", "cascode module connected to receive at its second current terminals ... a second output waveform", "engineering the resistive loads ... and said second output waveform" and "preconditioning the signal input applied to said differential pair module's control inputs" as recited in claim 14; the combination of "the cascode transistor module", "the differential pair module", "cascode module connected to receive at its second current terminals ... and a second output waveform", "engineering the resistive loads ... and said second output waveform" and "establishing a driving stage ... and engineering the output resistance of said driving stage" as recited in claim 16; the combination of "the cascode transistor module", "the differential pair module", "cascode module connected to receive at its second current

terminals .... and a second output waveform”, “engineering the resistive loads ... and said second output waveform” and “pair of external load impedances comprise one or more inductive modules” as recited in claim 21; the combination of “the cascode transistor module arranged to receive at its second current terminals substantially differential current signal from the first terminals of said differential pair module and to transmit at its first current terminals said substantially differential current signal into a pair of external load impedances as a first output waveform and a second output waveform”, “the resistive load comprising first and second resistances, said first resistance connected between the first terminal of one of said differential pair module transistors and the second terminal of one of said cascode module transistors, and said second resistance connected between the first terminal of the other of said differential pair module transistors and the second terminal of the other of said cascode module transistors” and “the cascode bias voltage node for applying a cascode bias voltage to the control inputs of said cascode transistor module transistors ...” as recited in claim 24; the combination of “the cascode transistor module ... as a first output waveform and a second output waveform”, “the resistive load ... and the second terminal of the other of said cascode module transistors”, “the cascode bias voltage node for applying a cascode bias voltage to the control inputs of said cascode transistor module transistors ...” and “one or more stages for preconditioning a differential input signal applied to said differential pair module’s control inputs” as recited in claim 37.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to My-Trang N. Ton whose telephone number is 571-272-1754. The examiner can normally be reached on 7:00 a.m - 5:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



MY-TRANG NUTON  
PRIMARY EXAMINER

September 1, 2004